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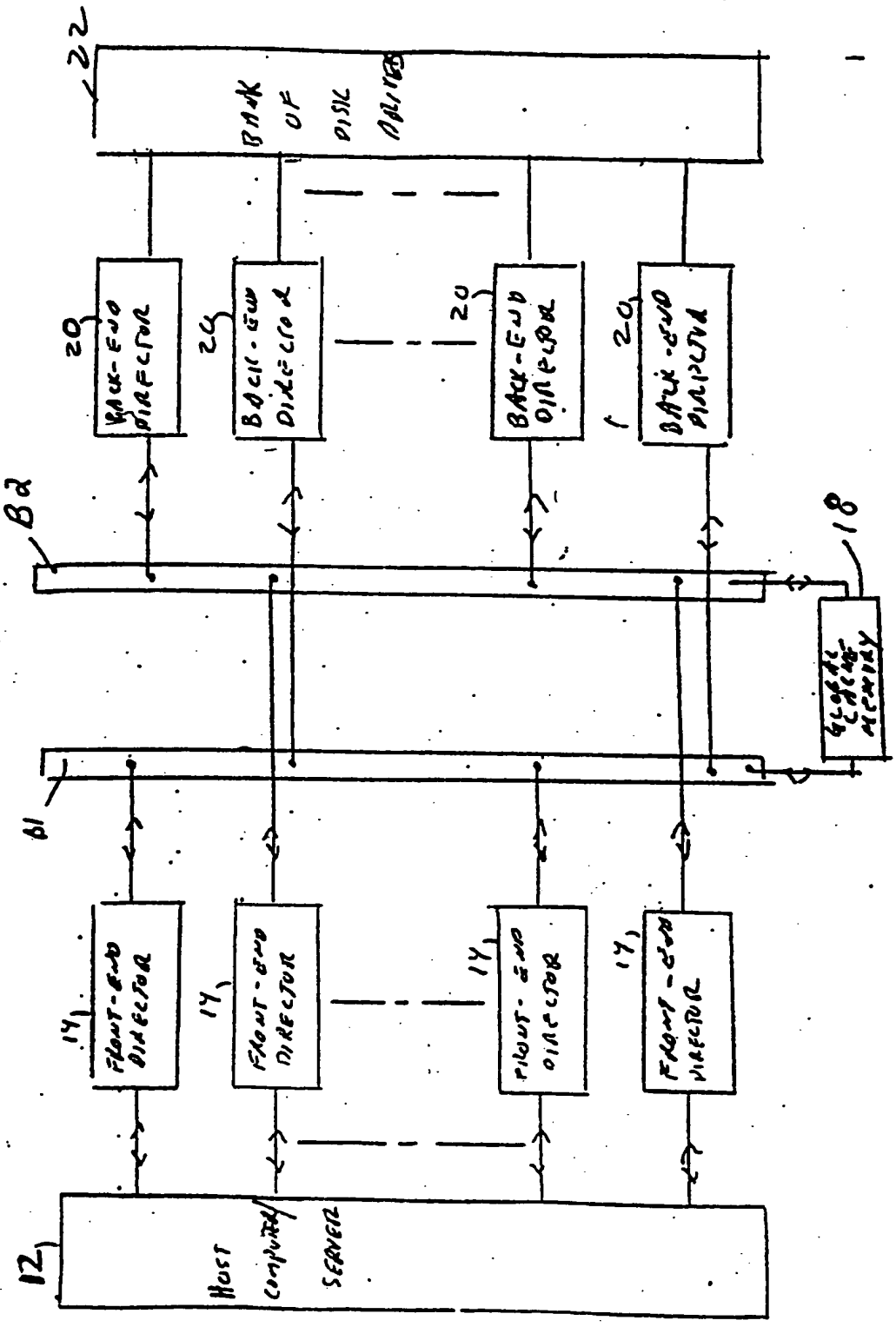


FIG. 1
PRIOR ART

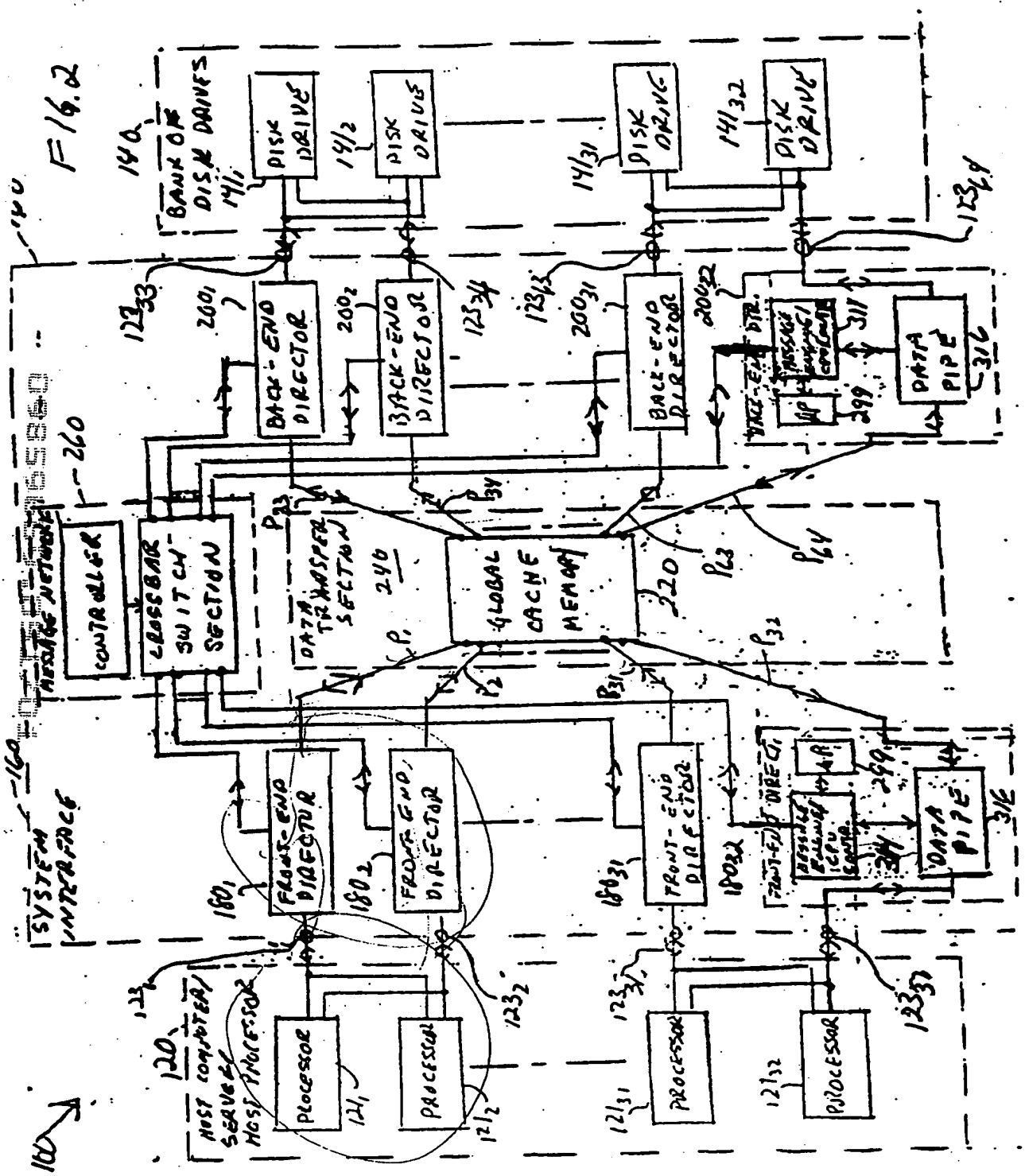


FIG. 2
100
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
121
PROCESSOR
123
SYSTEM INTERFACE
160
FRONT-END DIRECTOR
180
CONTROLLER
REMOTE NETWORK
CROSSBAR SWITCH SECTION
DATA TRANSFER SECTION
240
GLOBAL CACHE MEMORY
220
BACK-END DIRECTOR
200
DISK DRIVES
140
DISK DRIVE
141
DATA PIPE
316

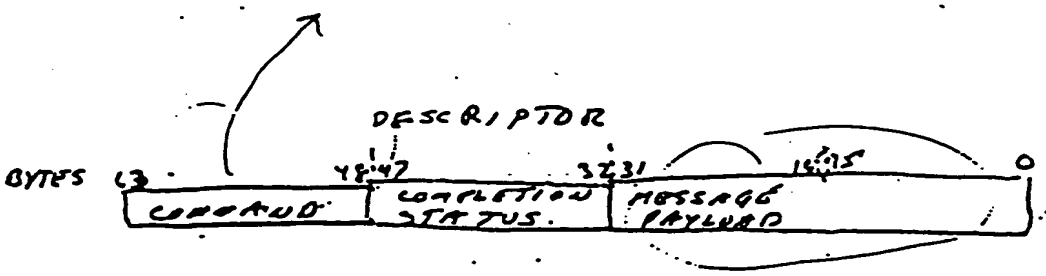

DESCRIPTOR
BYTES
63
31
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

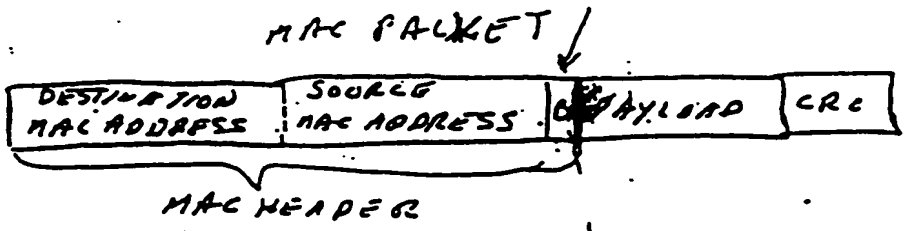

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

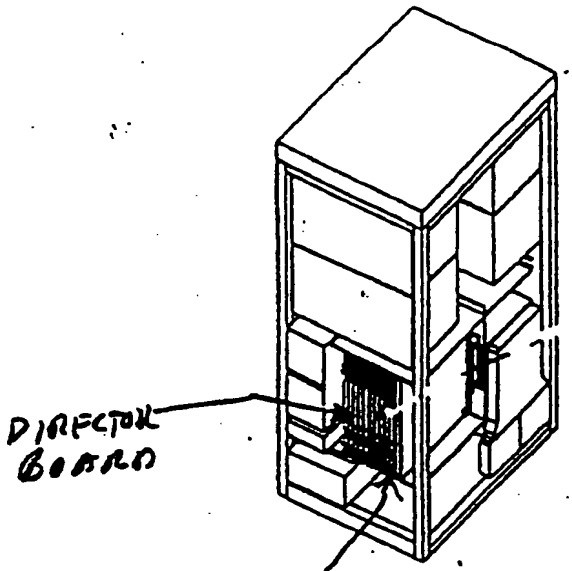
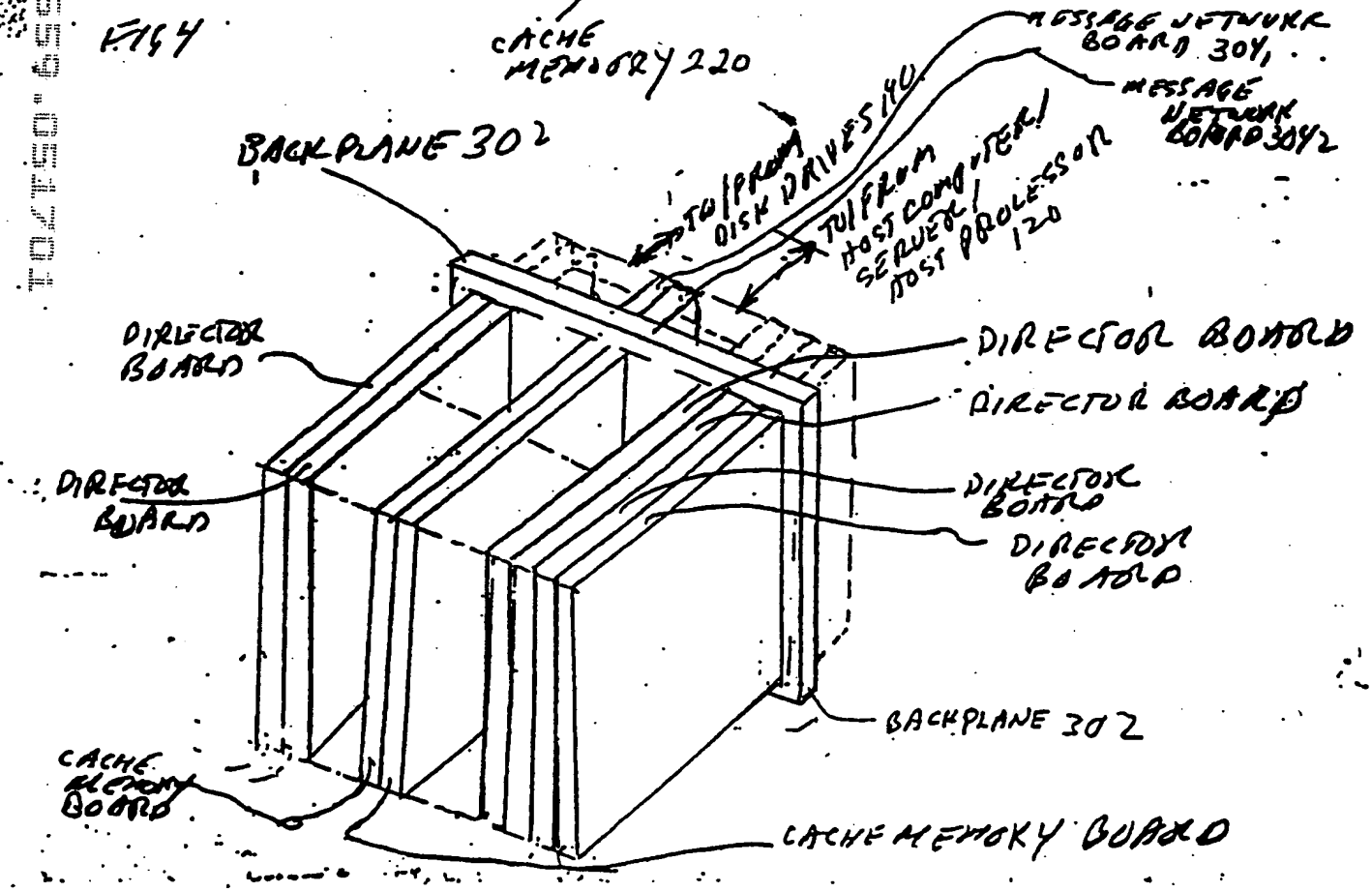

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304 2
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD

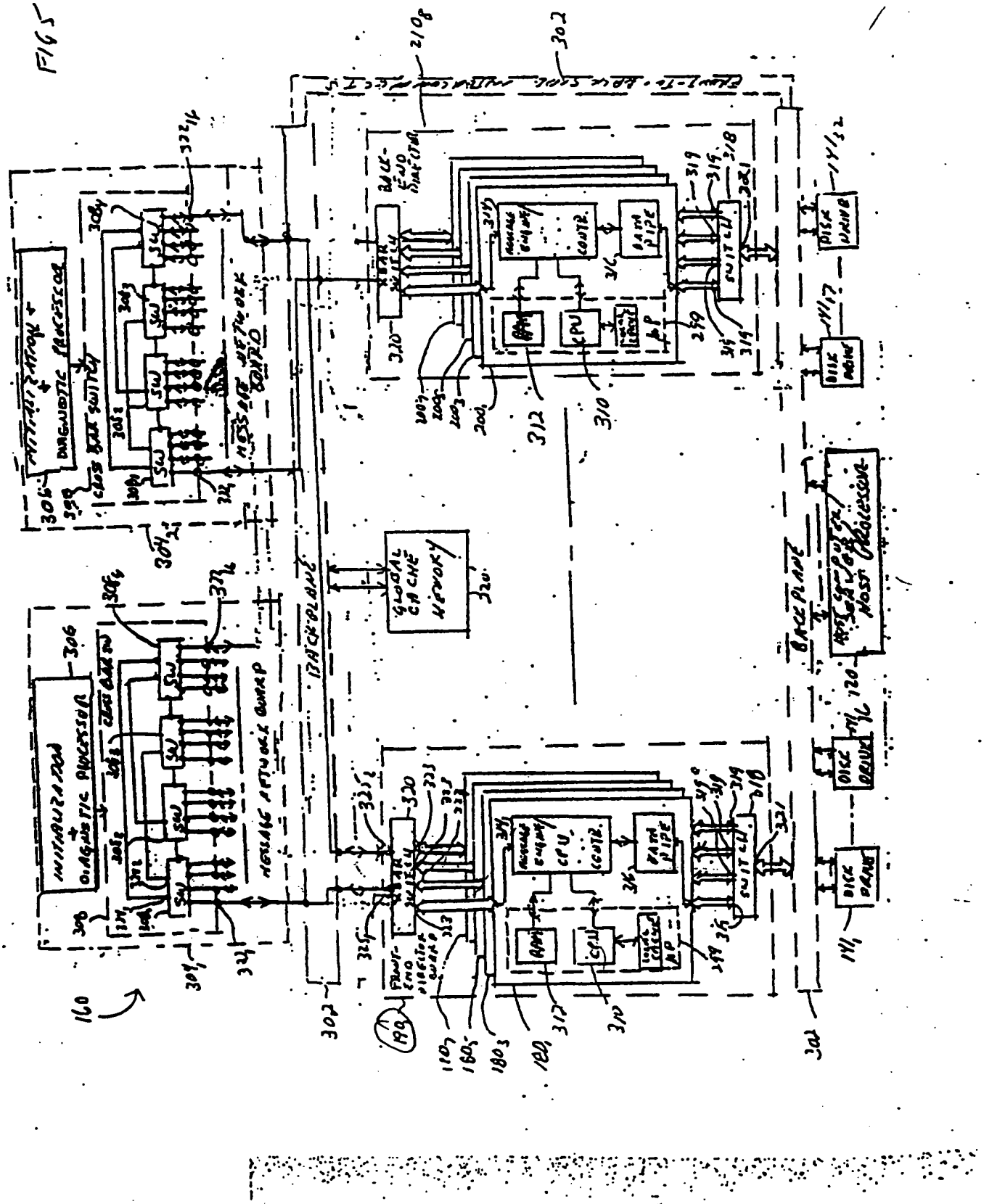


FIG 5
160
302
312
310
120
MESSAGE ACTIVATED SWITCH
GLOBAL CACHE MEMORY
DISC DRIVE
DISC PLANE
HOST ADAPTER
CPU
CACHE
PATH LOGIC
UNIT CTL
ADAPTER
PROCESSOR
DIAGNOSTIC PROCESSOR
SWITCH

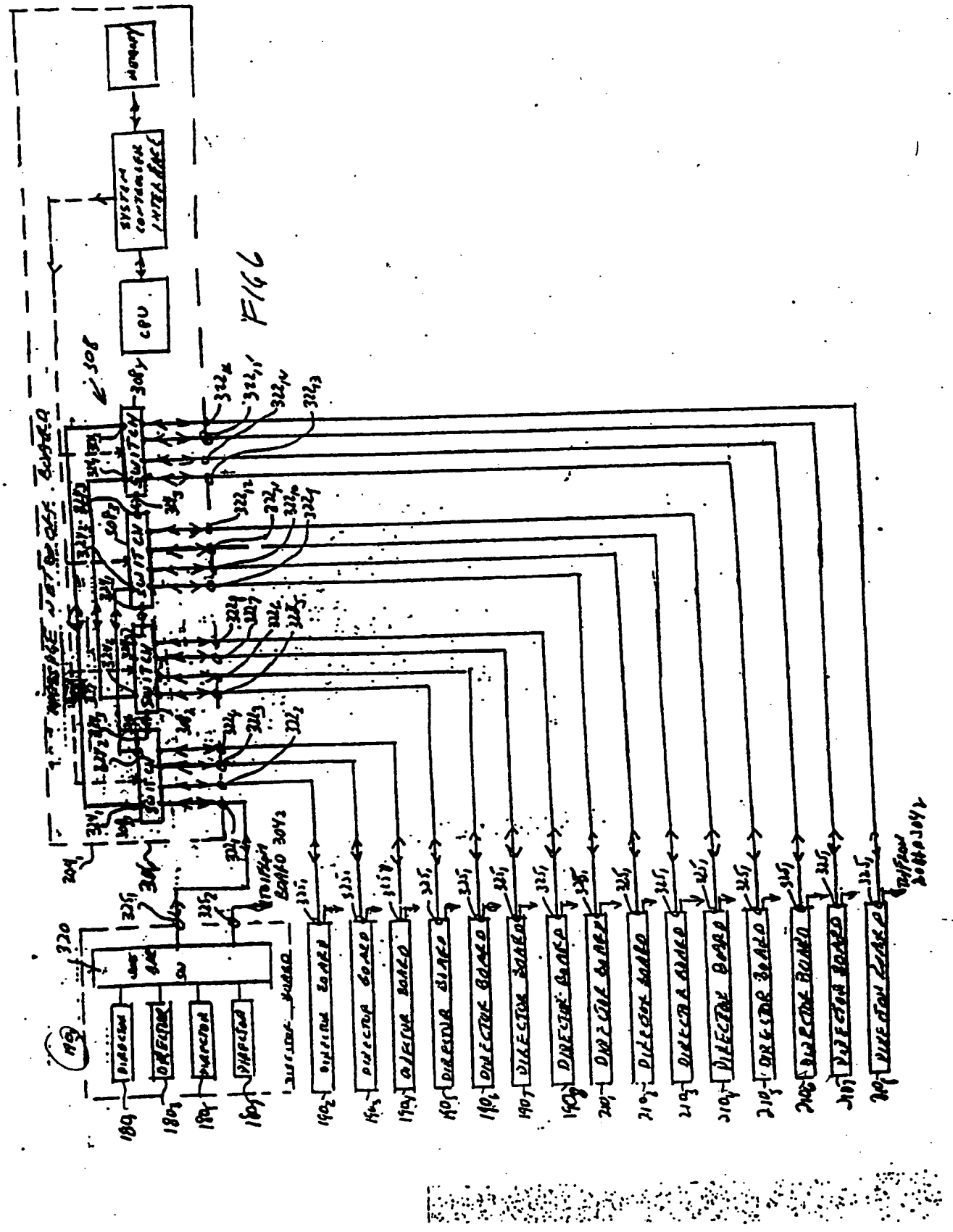
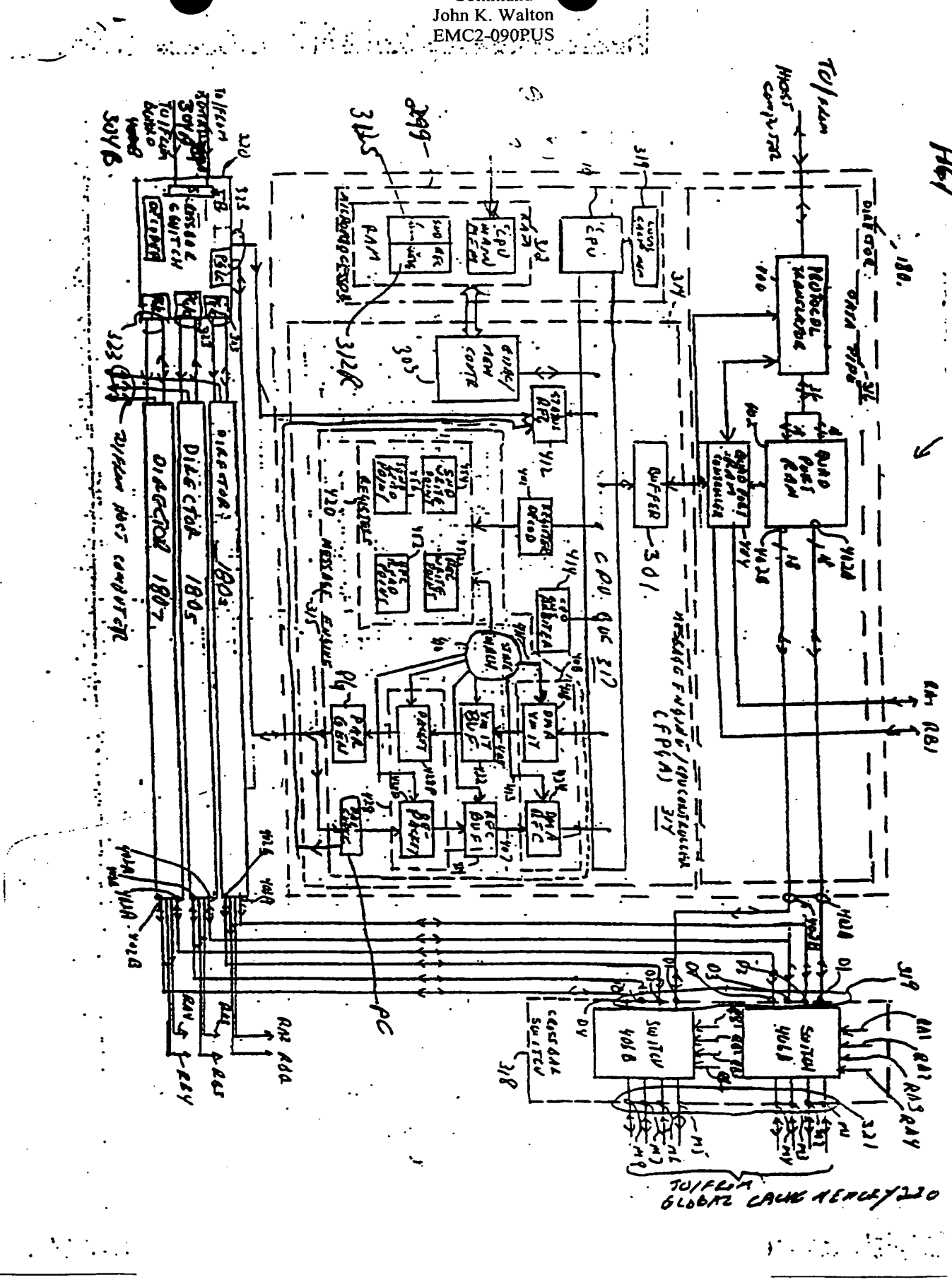


Fig 1

10/450,956



09090-0540

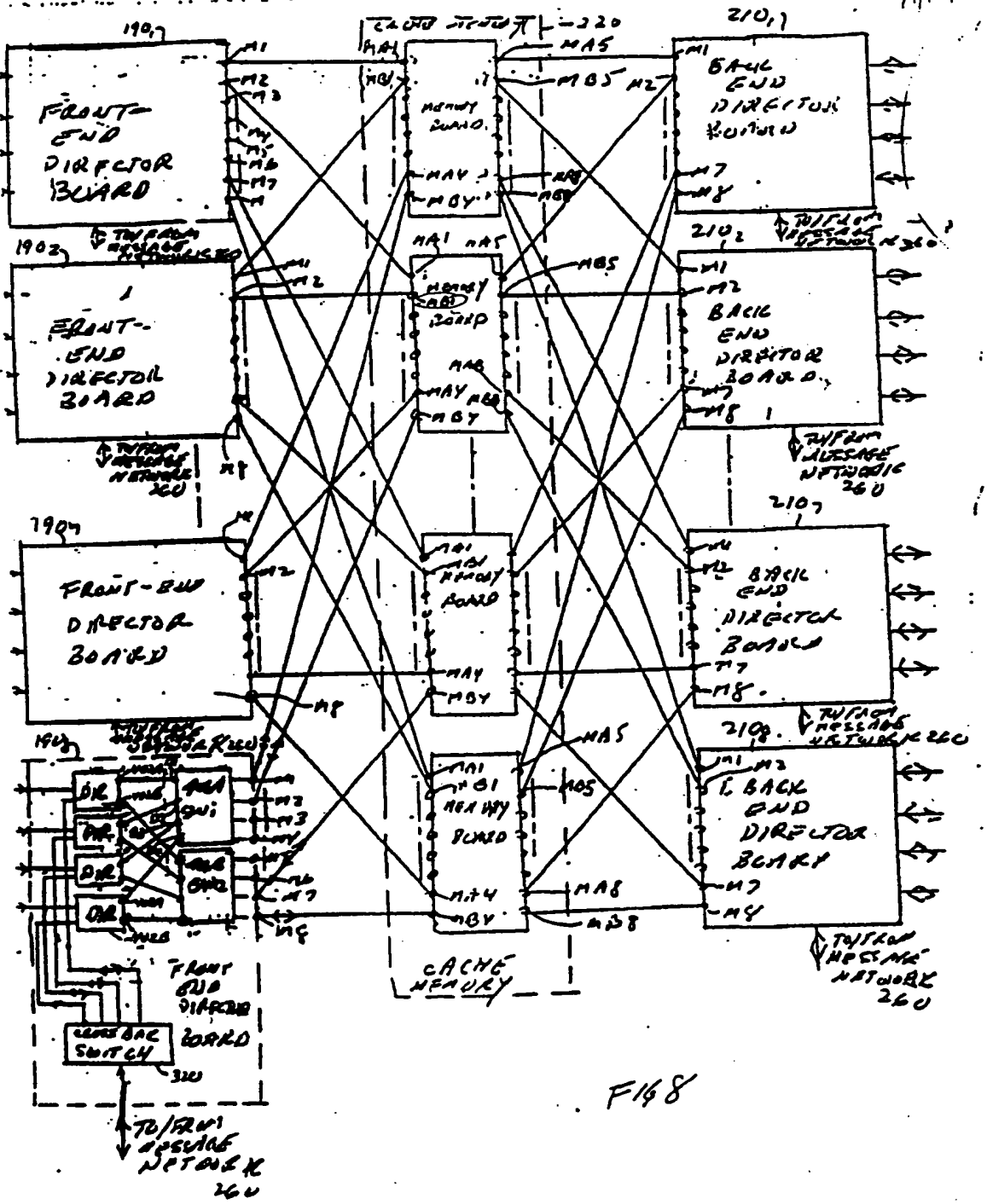

FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
SWITCH
TO/FROM HOST/DISK NETWORK 260

FIG 8

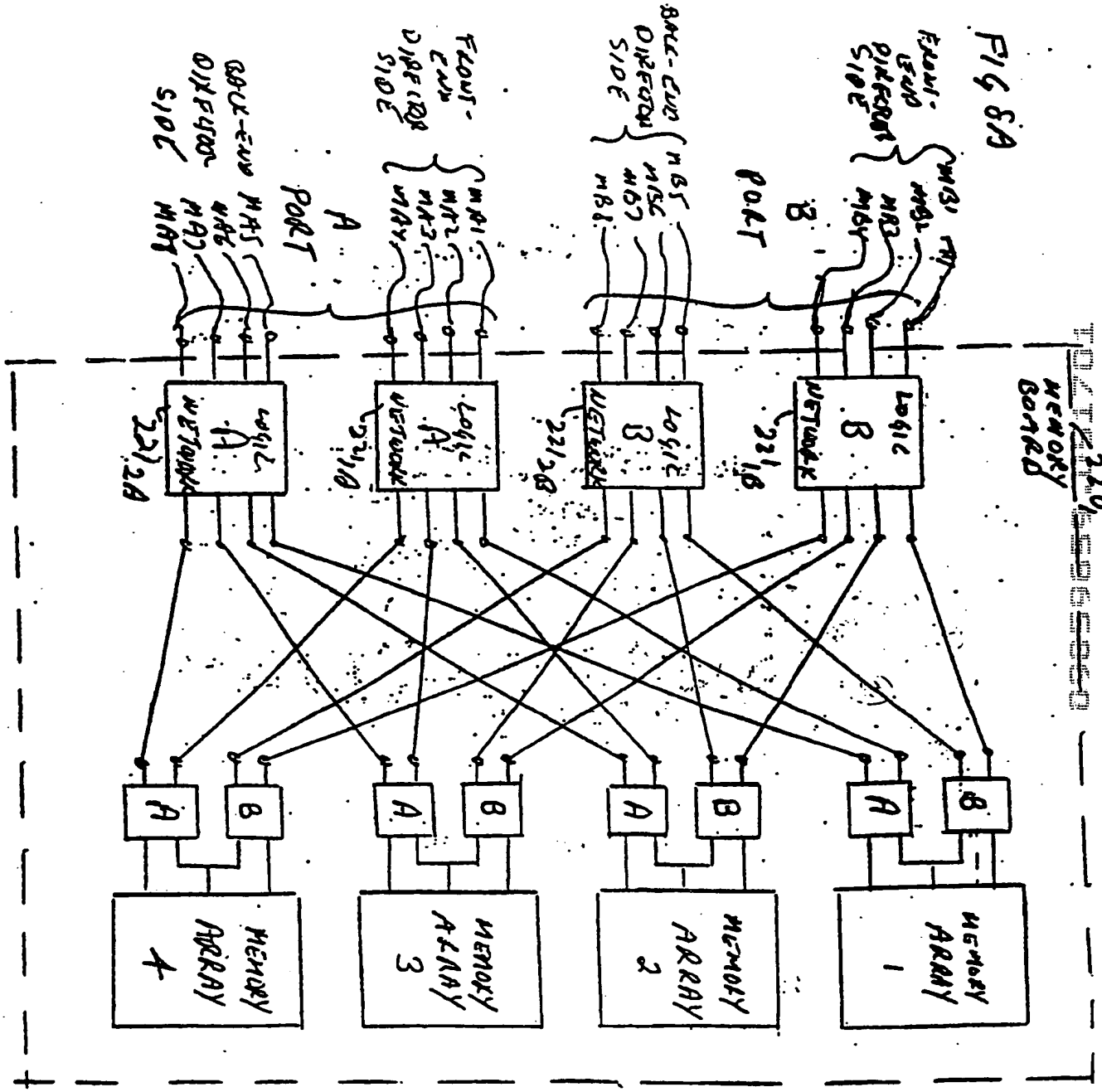


FIG 6A
MEMORY BOARD
220
B PORT
A PORT
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE
MBI
MB2
MB3
MB4
MB5
MB6
MB7
MB8
LOGIC B NETWORK
221B
LOGIC A NETWORK
221A
A
B
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4

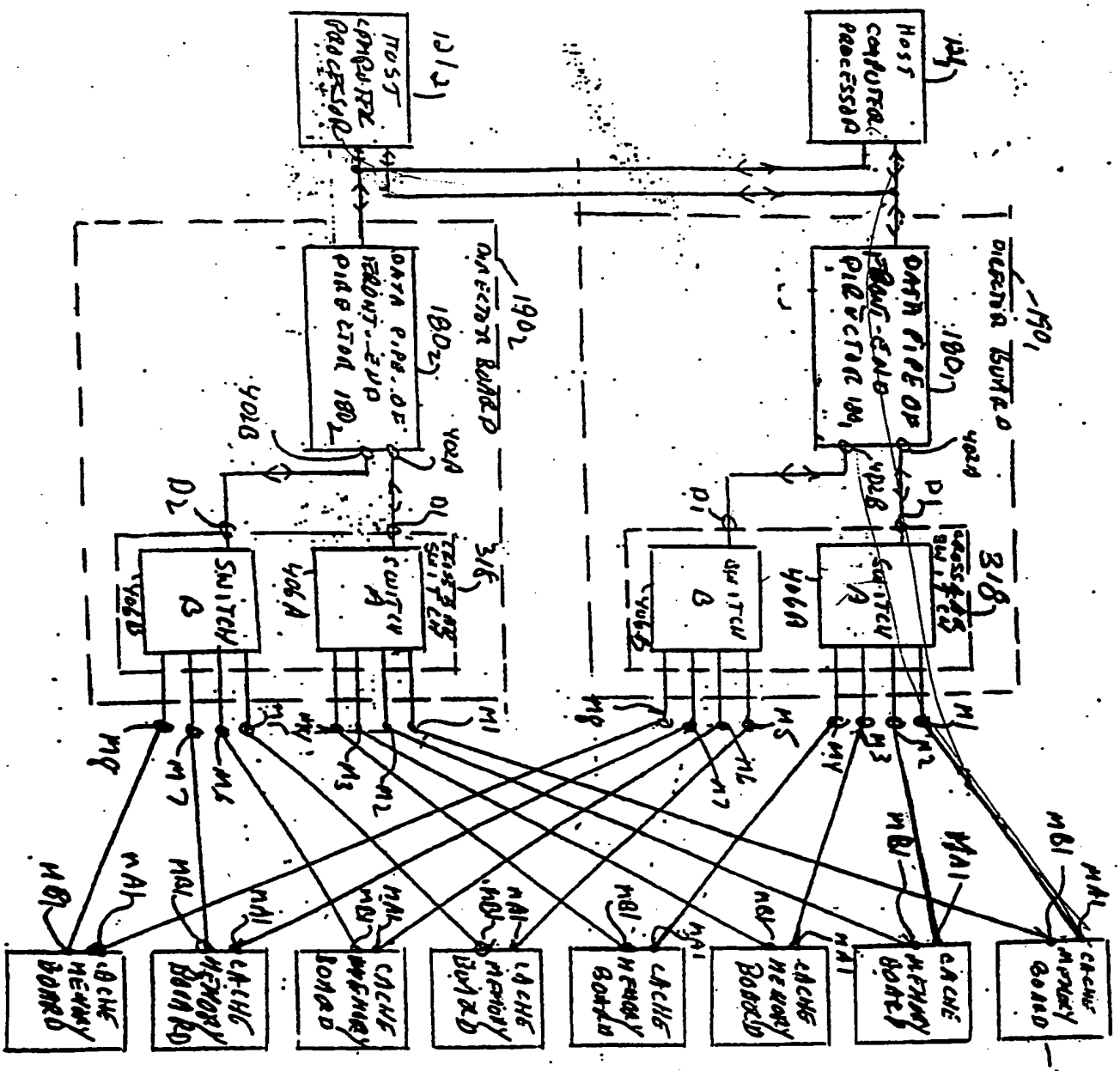
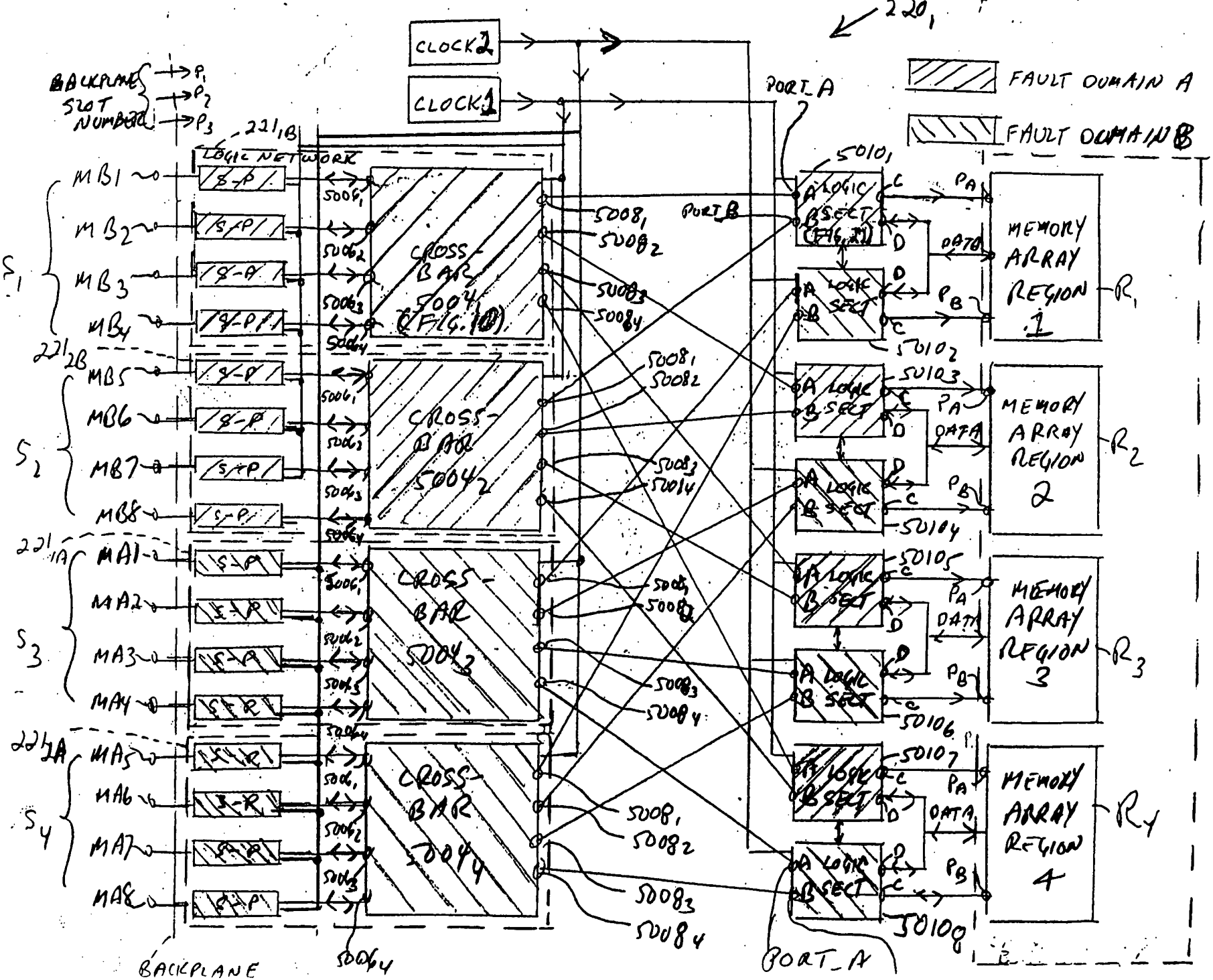

Host Computer Processor
Host Computer Processor
Data Pipe Director
Data Pipe Director
Director Board
Director Board
Cross-Bar Switch
Cross-Bar Switch
Switch A
Switch B
Switch A
Switch B
Cache Memory Board
Cache Memory Board
Cache Memory Board
Cache Memory Board
Cache Memory Board
Cache Memory Board
Cache Memory Board
Cache Memory Board
190
190
190
190
220
310
310
316
316
320
320
320
320
330
330
330
330
M0
M1
M2
M3
M4
M5
M6
M7
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MB0
MB1
MB2
MB3
MB4
MB5
MB6
MB7

FIG 8B

FIG. 9


220₁
CLOCK 2
CLOCK 1
BACKPLANE SLOT NUMBER
P1
P2
P3
221₁B
LOGIC NETWORK
MB1
MB2
MB3
MB4
S1
221₂B
MB5
MB6
MB7
MB8
S2
221₁A
MA1
MA2
MA3
MA4
S3
221₂A
MA5
MA6
MA7
MA8
S4
S/P
CROSS-BAR 5004 (FIG. 10)
CROSS-BAR 5004₂
CROSS-BAR 5004₃
CROSS-BAR 5004₄
5006₁
5006₂
5006₃
5006₄
5008₁
5008₂
5008₃
5008₄
PORT_A
PORT_B
FAULT DOMAIN A
FAULT DOMAIN B
5010₁
5010₂
5010₃
5010₄
5010₅
5010₆
5010₇
5010₈
A LOGIC B SECT (FIG. 11)
C
D
DATA
PA
PB
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
R1
R2
R3
R4
BACKPLANE
PORT_A

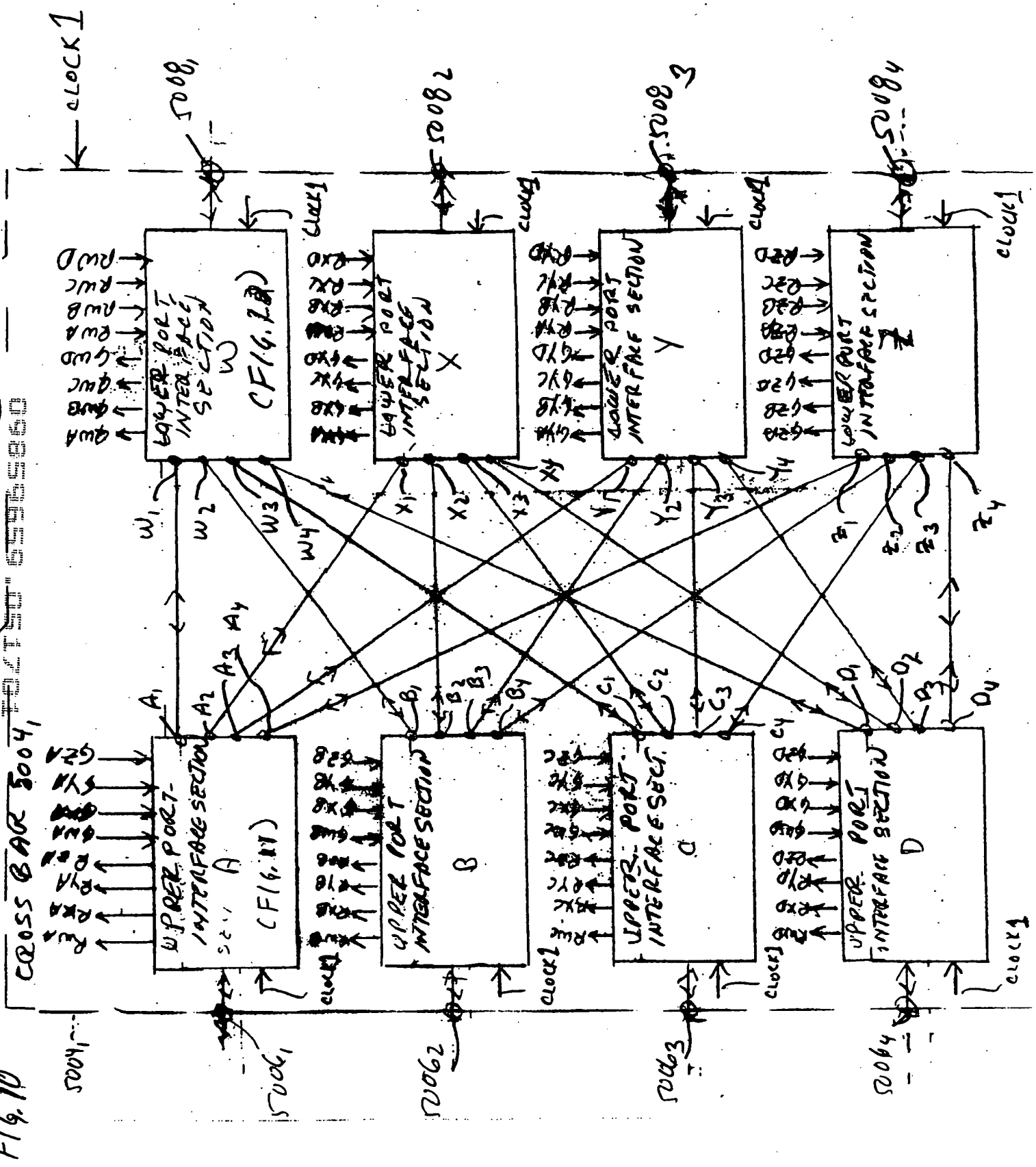

CROSS BAR SOC 1
CLOCK 1
SOC 1
SOC 2
SOC 3
SOC 4
LOWER PORT INTERFACE SECTION W (CFIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
UPPER PORT INTERFACE SECTION A (CFIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECTION C
UPPER PORT INTERFACE SECTION D

FIG. 10

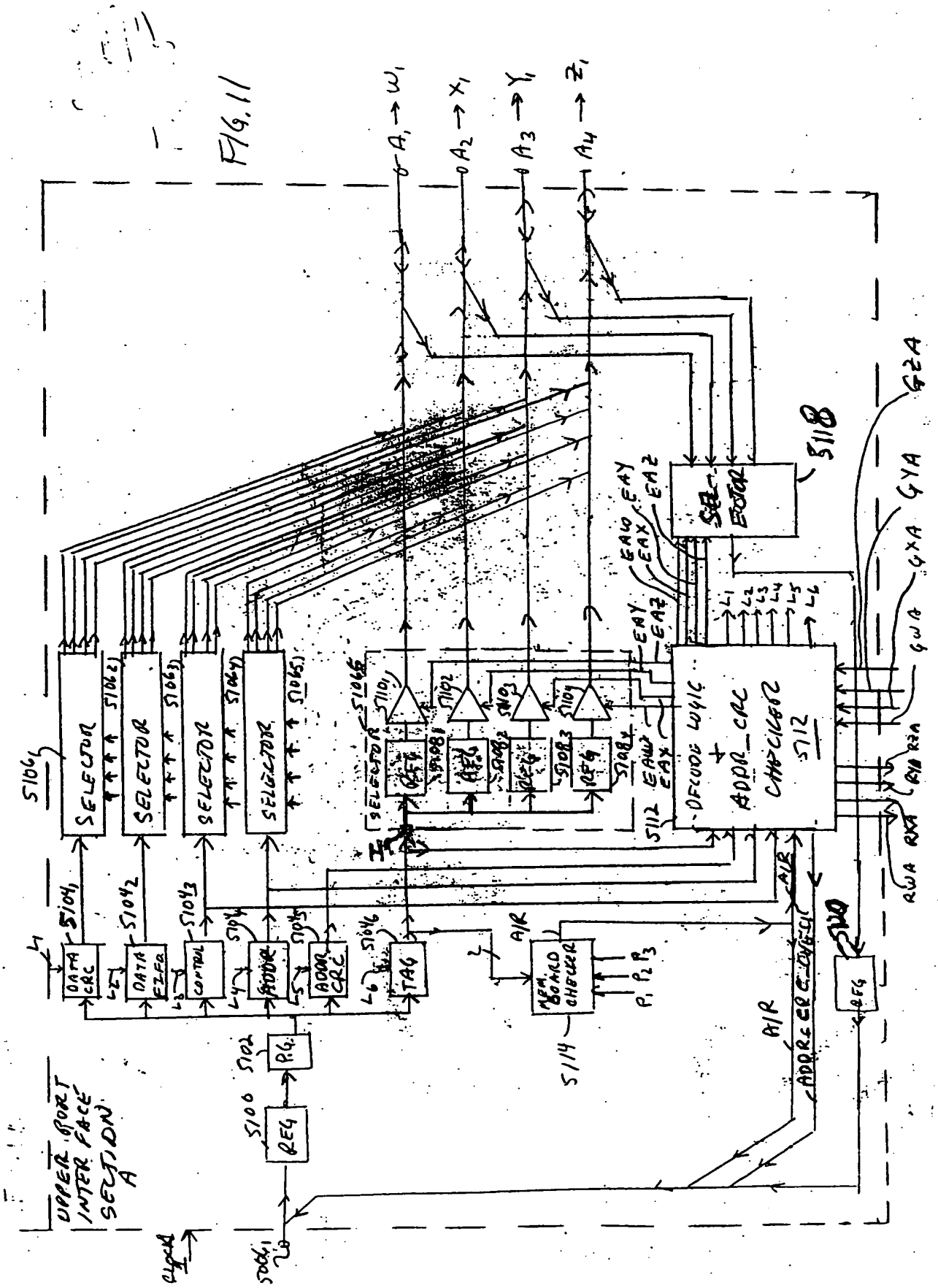
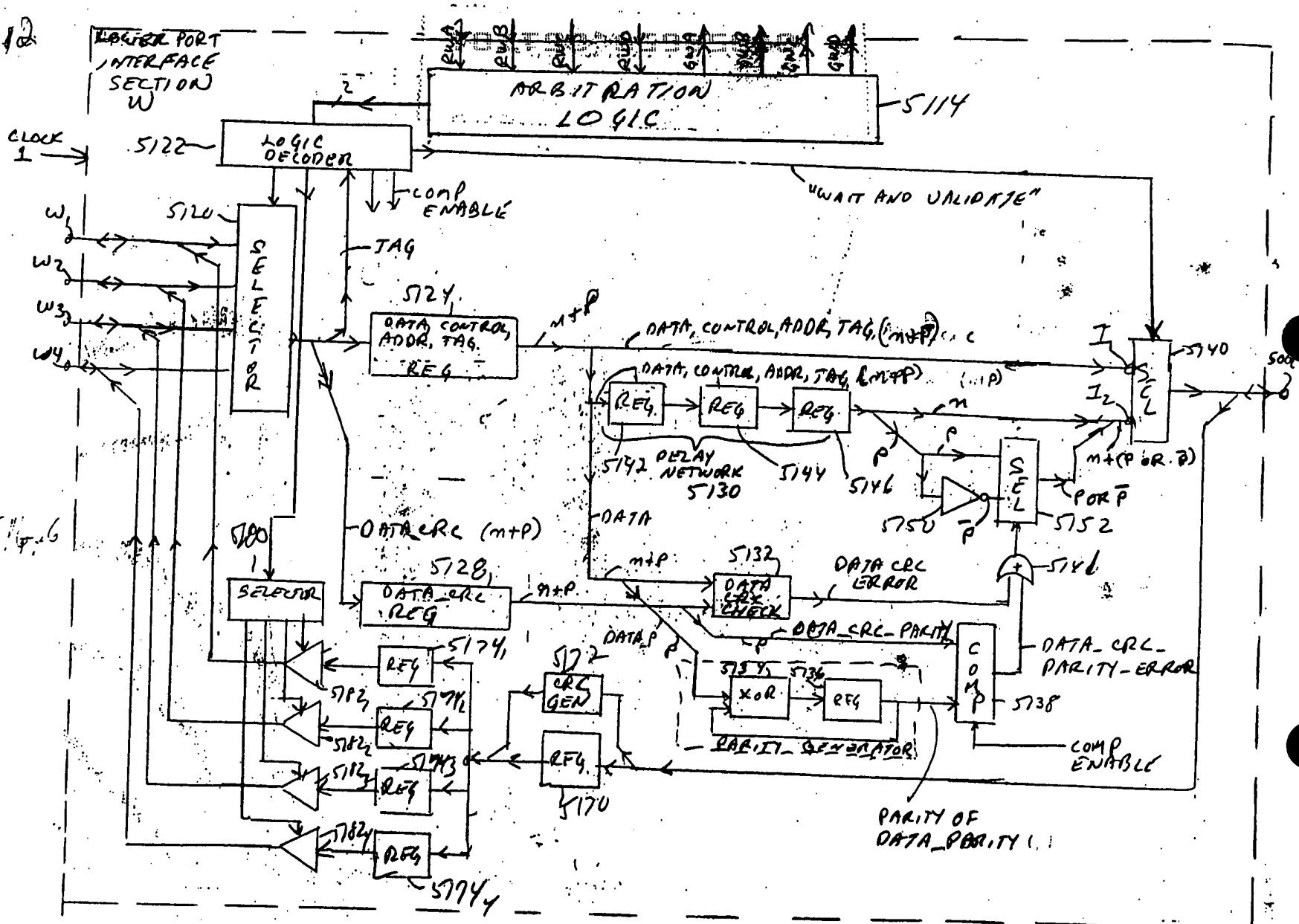


FIG. 11
UPPER PORT INTERFACE SECTION
SELECTOR
DATA CRC
DATA EZEA
CONTROL
ADDR
ADDR CRC
TAG
REG
DECODE LOGIC + ADDR_CRC CHECKER
SEL EDGE
DEG
REM BOARD CHECKER
ADDR_CRC GEN
A/R
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1

Data Storage System Having No-Operation Command
John K. Walton
EMC2-090PUS

FIG. 12



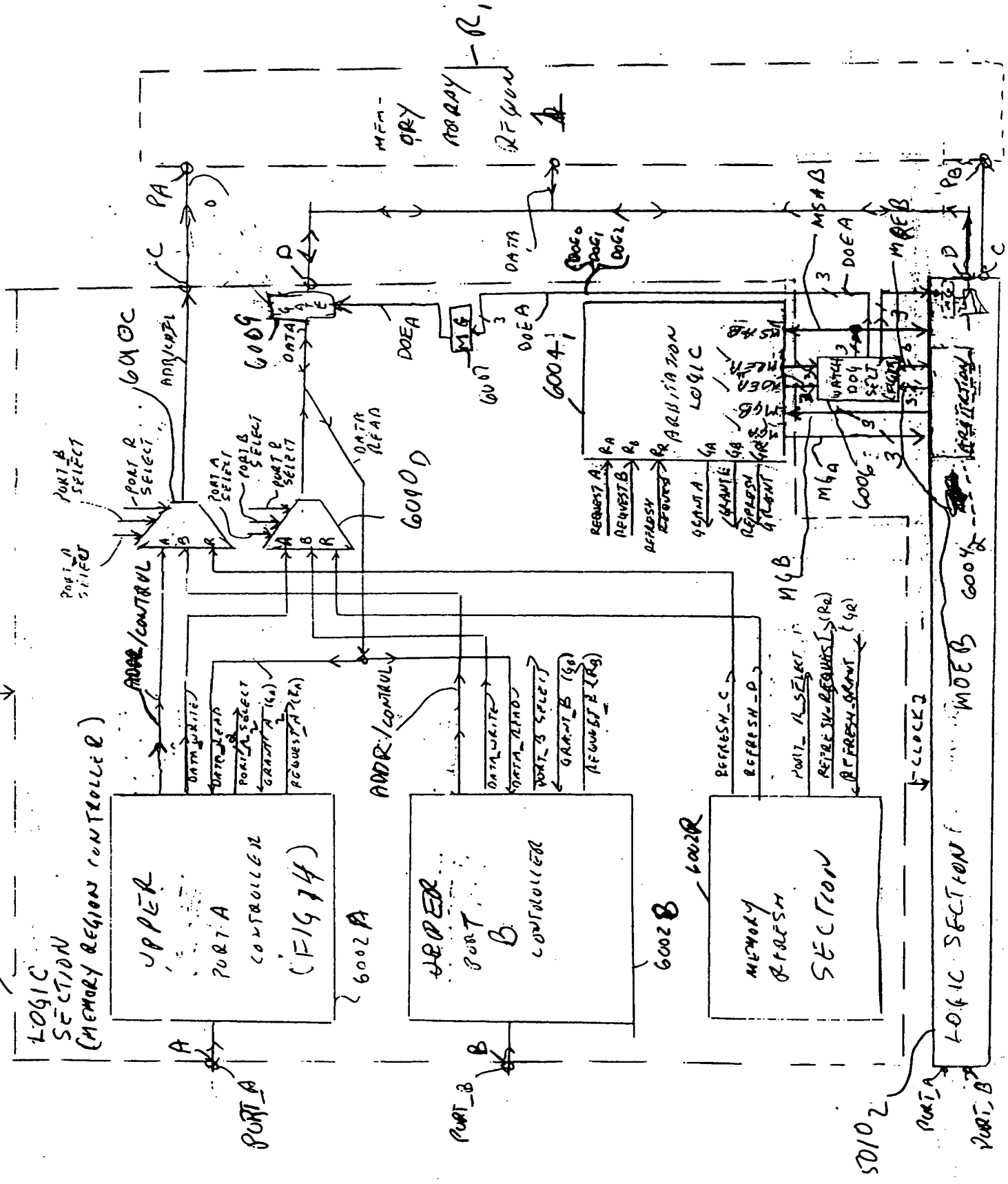

LOGIC SECTION (MEMORY REGION CONTROLLER)
5010
UPPER PORT A CONTROLLER (FIG 14)
6002A
UPPER PORT B CONTROLLER
6002B
MEMORY REFRESH SECTION
LOWER
MEM-ORY ARRAY REGION
6004
MODE
CLOCK
LOGIC SECTION
5010
PORT_A
PORT_B
ADDR/CONTROL
DATA
6009
6010
6004-1
ARBITRATION LOGIC
MUX
MATCH
REFRESH

FIG. 13

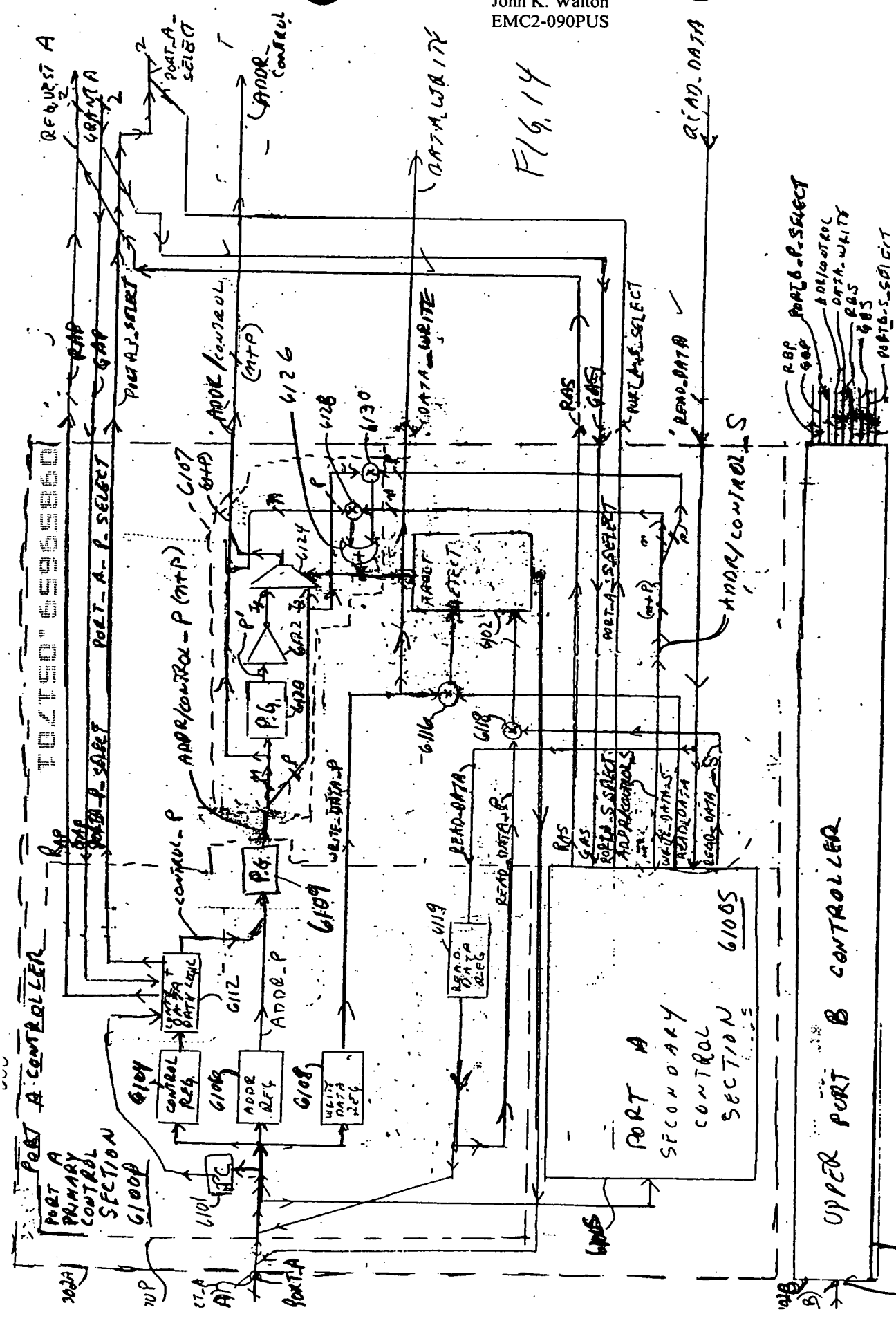


FIG. 14
PORT A CONTROLLER
PORT A PRIMARY CONTROL SECTION 6100A
PORT A SECONDARY CONTROL SECTION 6100S
UPPER PORT B CONTROLLER
PORT B
6102B
REQUEST A
GRANT A
PORT_A_SELECT
ADDR_control
DATA_WRITE
READ_DATA
RAS
CAS
PORT_A_P_SELECT
ADDR/control_P (mtp)
control_P
WRITE_DATA_P
ADDR_P
READ_DATA_P
ADDR/control_S
PORT_A_S_SELECT
WRITE_DATA_S
READ_DATA_S
RBP
RBS
GBS
PORT_B_SELECT
6104
6106
6108
6109
6110
6112
6114
6116
6118
6119
6120
6122
6124
6126
6128
6130
6102
6107
6101

Data Storage System Having No-Operation Command
John K. Walton
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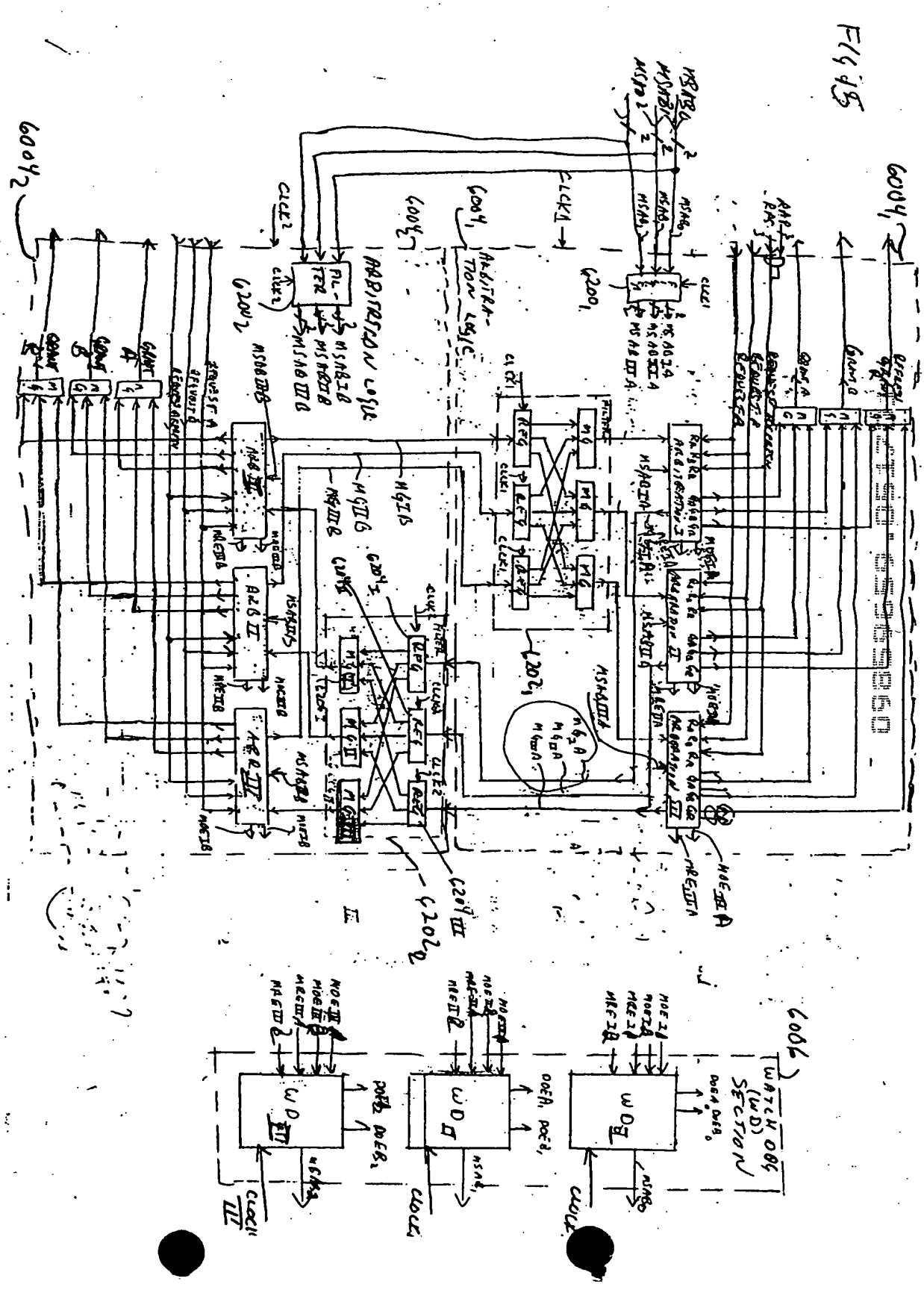


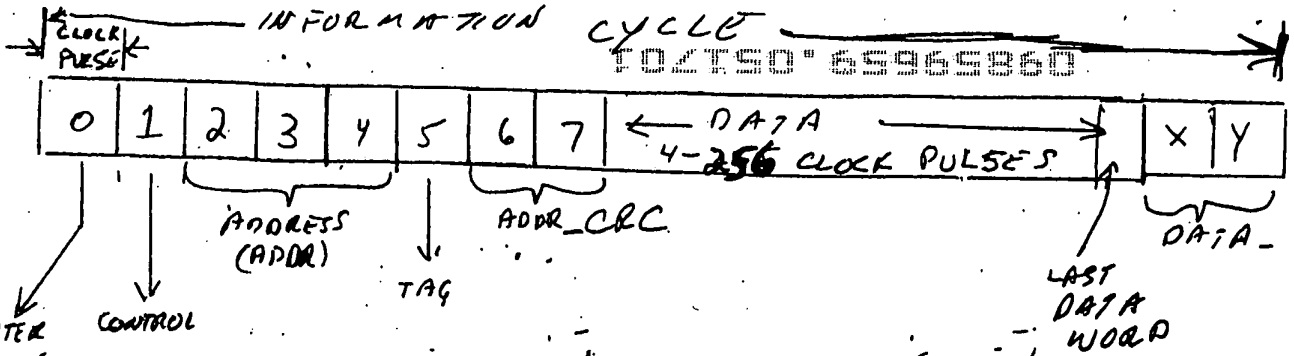


FIG. 16

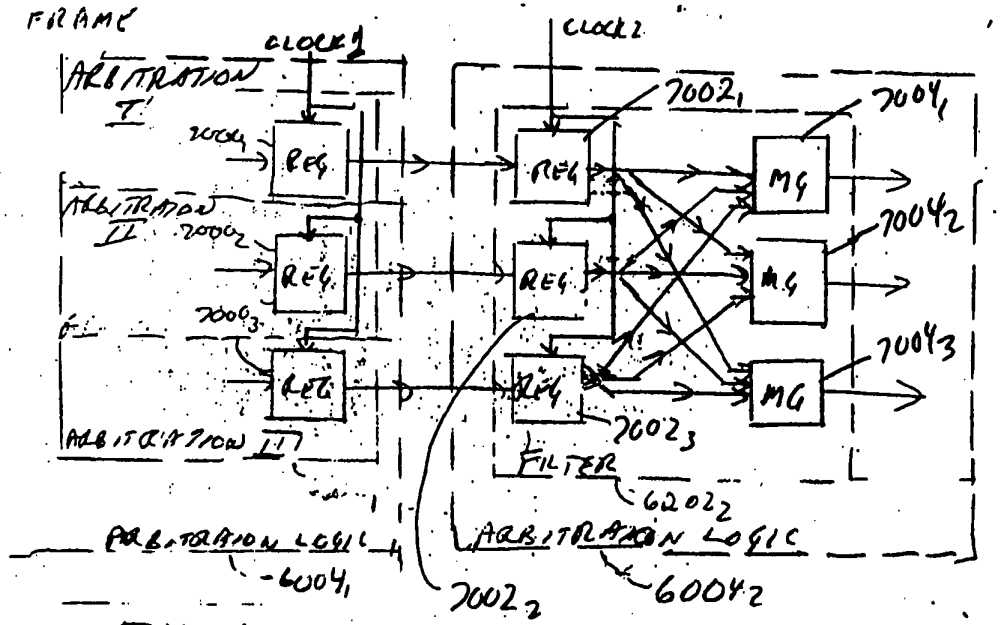


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

FIG. 19

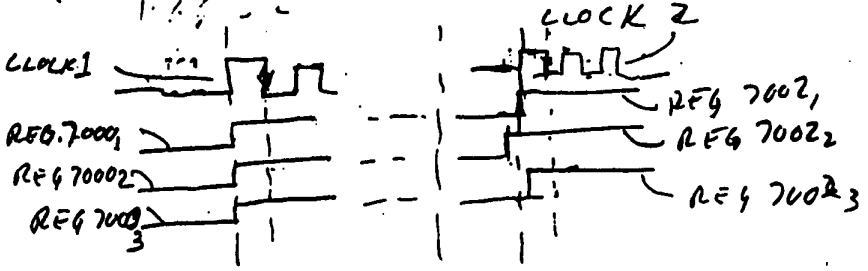
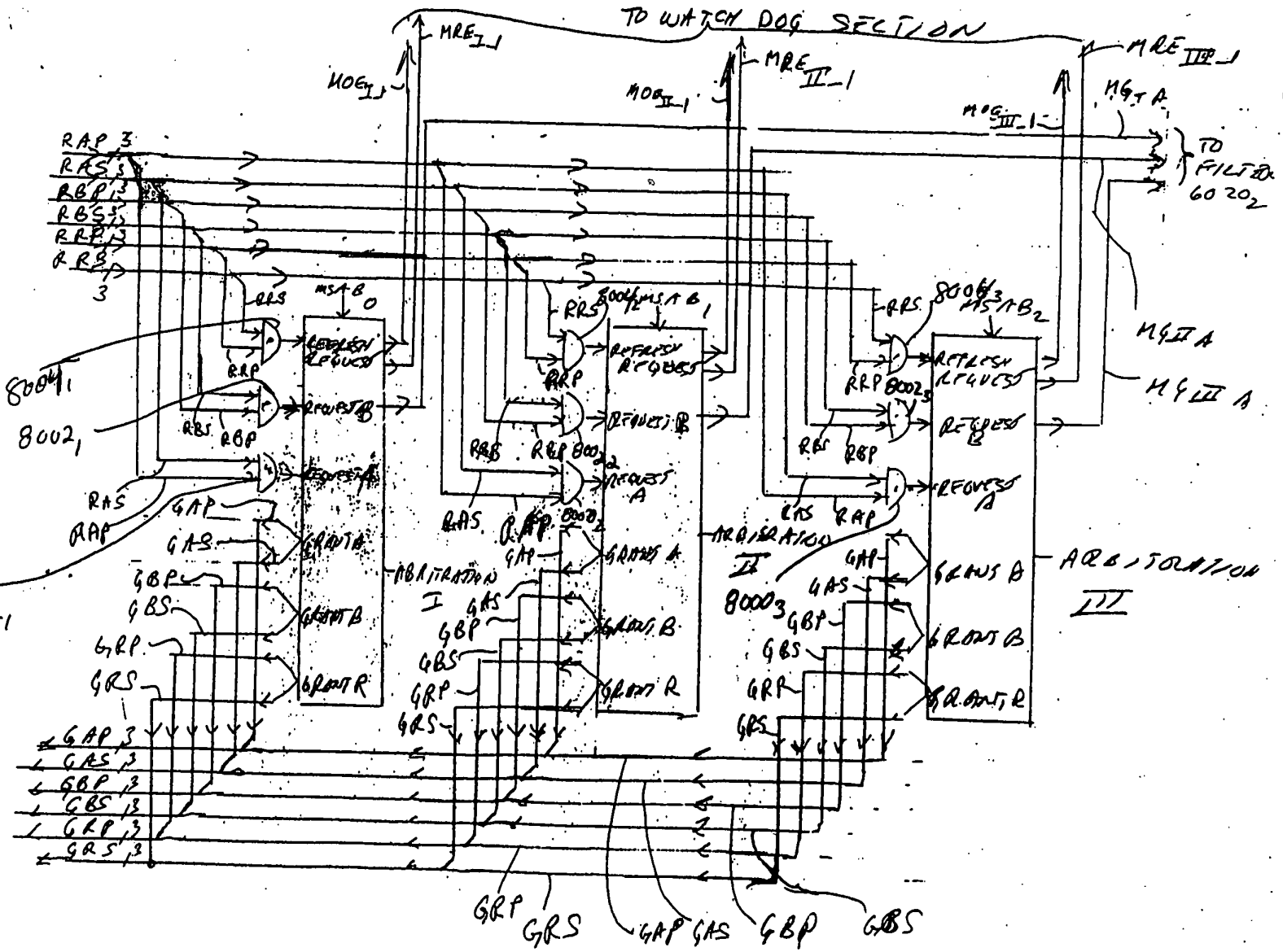


Fig. 20


TO WATCH DOG SECTION
MRE I_1
MRE II_1
MRE III_1
MOG I_1
MOG II_1
MOG III_1
MG I A
TO FILTER 60 20₂
MG II A
MG III A
RAP 3
RAS 3
RBP 3
RBS 3
RRP 3
RRS 3
8000₁
8002₁
8000₂
8002₂
8000₃
8002₃
MSAB 0
MSAB 1
MSAB 2
ARBITRATION I
ARBITRATION II
ARBITRATION III
GAP 3
GAS 3
GBP 3
GBS 3
GRP 3
GRS 3
GRP
GRS
GAP
GAS
GBP
GBS